

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
Yuuichi MIKATA et al.) Parent Group Art Unit: 2815
)
Application No.: 1.53(b) Divisional of) Parent Examiner: Eckert II, George C.
Application No. 09/459,913, filed)
December 14, 1999)
)
Application No.: To be Assigned)
)
Filed: Herewith)
)
For: RELIABLE SEMICONDUCTOR)
DEVICE AND METHOD OF)
MANUFACTURING THE SAME)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicants bring to the attention of the Examiner the documents listed on the attached PTO 1449. This Information Disclosure Statement (IDS) is being filed concurrently with the above-referenced divisional application.

The listed documents were previously submitted in an IDS or cited by the Examiner in a prior application, Application No. 09/459,913, filing date December 14, 1999, upon which Applicants rely for the benefits provided in 35 U.S.C. § 120. Applicants respectfully request that the Examiner consider the listed documents and

indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and Applicants determine that the cited documents do not constitute "prior art" under United States law, Applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents.

Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 11, 2004

By:  Reg 24,014
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INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.2204-01	Appln. No.	
Applicant	Yuuichi MIKATA et al.		
Filing Date	Herewith	Group:	

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		5,786,027	Jul. 28, 1998	Rolfson			
		5,767,004	Jun. 16, 1998	Balasubramanian et al.			
		5,753,134	May 19, 1998	Biebl			
		5,354,702	Oct. 11, 1994	Arima et al.			
		4,745,088	May 17, 1988	Inoue et al.			
		5,150,178	Sep. 1992	Mori			
		4,295,265	Oct. 1981	Horiuchi et al.			
		5,759,883	Jun. 1998	Kinoshita			
		4,910,163	Mar. 20, 1990	Jain			
		4,745,079	May 1988	Pfiester			
		5,360,756	Nov. 1994	Tamura			
		5,831,694	Nov. 1998	Onisawa et al.			
		5,990,517	Nov. 1999	Irino			
		5,999,236	Dec. 1999	Nakajima et al.			
		6,069,061	May 2000	Lin et al.			
		6,118,140	Sep. 2000	Nakamima et al.			

Examiner	Date Considered
<p>*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>	
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Applicant	Yuuichi MIKATA et al.		
Filing Date	Herewith	Group:	

FOREIGN PATENT DOCUMENTS						
	Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
	03163874	Jul. 15, 1991	Japan			English Abstract
	9-246206	Sep. 19, 1997	Japan			English Abstract
	63042174	Feb. 23, 1988	Japan			English Abstract
	08321612	Dec. 3, 1996	Japan			English Abstract
	3-62-033470	Feb. 1987	Japan			
	3-62-037160	Feb. 1987	Japan			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Copy of European Search Report dated May 22, 2001.
	Miura, H. et al., "Effect of Mechanical Stress on Reliability of Gate-Oxide Film in MOS Transistors", INTERNATIONAL ELECTRON DEVICES MEETING, TECHNICAL DIGEST (Cat. No. 96CH35961), San Francisco, CA, pp. 743-746, 12/1996
	Hamada et al., A New Aspect on Mechanical Stress Effects in Scaled MOS Devices, 1990, IEEE, Symposium on VLSI Technology, pp. 113-14
	Hamada et al., Hot-Electron Trapping Activation Energy in PMOSFET's Under Mechanical Stress, Jan. 1994, IEEE, Electron Device Letters, Vol. 15, No. 1, pp. 31-32.

Examiner	Date Considered
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